AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows. Please add new claims 18-20.

1. (Currently Amended) A clustered computer system comprising:

a plurality of CPU and memory installed ~~apparatus each~~ apparatuses having at least one CPU and at least one memory[[,]]; and

a plurality of input/output control ~~apparatus~~ apparatuses,

wherein said CPU and memory installed ~~apparatus~~ apparatuses and said input/output control ~~apparatus being~~ apparatuses are connected to each other by a network.

2. (Currently Amended) A computer system comprising:

a plurality of CPU and memory installed ~~apparatus each~~ apparatuses having at least one CPU and at least one memory[[,]];

a plurality of input/output control ~~apparatus,~~ apparatuses; and

a network connecting said CPU and memory installed ~~apparatus~~ apparatuses and said input/output control ~~apparatus~~ apparatuses to each other,

wherein each of said CPU and memory installed ~~apparatus~~ apparatuses ~~having~~ comprises communication means for transmitting an input/output instruction issued by ~~said~~ at least one CPU of ~~an own~~ said plurality of CPU and memory installed ~~apparatus~~ apparatuses to at least one of said input/output control ~~apparatus~~ apparatuses assigned in advance to ~~the own~~ said at least one CPU and memory installed ~~apparatus~~ apparatuses via said network, and ~~receiving~~ receives a response from at least one of said input/output control ~~apparatus~~

apparatuses via said network, and

wherein each of said input/output control ~~apparatus~~ apparatuses ~~having~~ comprises communication means for receiving an input/output instruction from ~~said~~ at least one CPU and memory installed ~~apparatus~~ apparatuses assigned in advance to ~~an own~~ at least one of said plurality of input/output control ~~apparatus~~ apparatuses via said network, and ~~transmitting~~ transmits a response to said input/output instruction to said at least one CPU and memory installed ~~apparatus~~ apparatuses via said network.

3. (Currently Amended) A computer system according to claim 2, wherein said communication means of each of said input/output control ~~apparatus~~ apparatuses comprises:

means for receiving ~~an~~ the input/output instruction as being effective only when the source of the input/output instruction received via said network is a CPU and memory installed ~~apparatus~~ apparatuses which has been set in advance.

4. (Currently Amended) A computer system according to claim 2, wherein said communication means of each of said CPU and memory installed ~~apparatus~~ apparatuses comprises:

means for receiving a response as being effective only when the source of the response received via said network is an input/output control ~~apparatus~~ apparatuses which has been set in advance.

5. (Original) A computer system according to claim 2, wherein said network is also used for communications between said plurality of CPU and memory installed

apparatus.

6. (Currently Amended) A computer system according to claim 3, wherein said communication means of each of said CPU and memory installed ~~apparatus~~ apparatuses comprises:

means for receiving a response as being effective only when the source of the response received via said network is an input/output control ~~apparatus~~ apparatuses which has been set in advance.

7. (Currently Amended) A computer system according to claim 5, wherein said communication means of each of said CPU and memory installed ~~apparatus~~ apparatuses comprises:

means for communicating with other CPU and memory installed ~~apparatus~~ apparatuses via said network.

8. (Currently Amended) A computer system according to claim 7, wherein the communications between said plurality of CPU and memory installed ~~apparatus~~ apparatuses are communications for accessing memories installed on other CPU and memory installed apparatus.

9. (Currently Amended) A computer system according to claim 2, further comprising:

means for, when either one of said CPU and memory installed ~~apparatus~~ apparatuses

fails to operate due to a fault, assigning said input/output control ~~apparatus~~ apparatuses which has been used by ~~the~~ a faulty CPU and memory installed ~~apparatus~~ apparatuses to another normal CPU and memory installed ~~apparatus~~ apparatuses hereby to continue system operation.

10. (Currently Amended) A computer system according to claim 9, wherein an active one of the CPU and memory installed ~~apparatus~~ apparatuses which is using another input/output control ~~apparatus~~ apparatuses is used as said other normal CPU and memory installed apparatus.

11. (Currently Amended) A computer system according to claim 9, further comprising:

a backup CPU and memory installed apparatus, said backup CPU and memory installed ~~apparatus~~ apparatuses being used as said other normal CPU and memory installed apparatus.

12. (Currently Amended) A computer system according to claim 2, further comprising:

at least one backup input/output control apparatus, and means for, when either active one of said input/output control ~~apparatus~~ apparatuses fails to operate due to a fault, assigning said backup input/output control ~~apparatus~~ apparatuses to said CPU and memory installed ~~apparatus~~ apparatuses which has been using the faulty input/output control ~~apparatus~~ apparatuses thereby to continue system operation.

13. (Currently Amended) A computer system comprising:

a CPU and memory installed ~~apparatus~~ apparatuses ~~having~~ comprising at least one CPU and at least one memory[[,]];

an input/output control apparatus[[,]]; and

a communication cable connecting said CPU and memory installed ~~apparatus~~ apparatuses and said input/output control ~~apparatus~~ apparatuses to each other,

wherein said CPU and memory installed ~~apparatus~~ apparatuses ~~having~~ comprises communication means for transmitting an input/output instruction issued by said CPU to said input/output control ~~apparatus~~ apparatuses via said communication cable, and ~~receiving~~ receives a response from said input/output control ~~apparatus~~ apparatuses via said communication cable, and

wherein said input/output control ~~apparatus~~ apparatuses ~~having~~ comprising communication means for receiving an input/output instruction from said CPU and memory installed ~~apparatus~~ apparatuses via said communication cable, and ~~transmitting~~ transmits a response to said input/output instruction to said CPU and memory installed ~~apparatus~~ apparatuses via said communication cable.

14. (Currently Amended) A CPU and memory installed ~~apparatus~~ apparatuses comprising:

at least one CPU and at least one memory[[,]];

communication means for communicating with an external circuit comprising an input/output control apparatus, transmitting an input/output instruction issued by said CPU to

~~an~~ said input/output control ~~apparatus~~ apparatuses which has been assigned in advance, and receiving a response from said input/output control apparatus[[,]]; and

a single board on which said CPU, said memory, and said communication means are mounted.

15. (Currently Amended) A CPU and memory installed ~~apparatus~~ apparatuses according to claim 14, wherein said communication means ~~has~~ comprises:

means for receiving said response as being effective only when the source of the received response is the input/output control ~~apparatus~~ apparatuses which has been assigned in advance.

16. (Currently Amended) An input/output control apparatus comprising:

an input/output control circuit for controlling a peripheral device based on an input/output instruction[[,]]; and

communication means for communicating with an external circuit comprising a CPU and memory installed apparatus, for receiving an input/output instruction from [[a]] said CPU and memory installed apparatus which has been set in advance and transferring said input/output instruction to said input/output control circuit, and for transmitting a response to said input/output instruction to said CPU and memory installed apparatus.

17. (Currently Amended) An input/output control apparatus according to claim 16, wherein said communication means ~~has~~ comprises:

means for receiving said input/output instruction as being effective only when the

source of the received input/output instruction is the CPU and memory installed apparatus which has been set in advance.

18. (New) A computer system according to claim 2, wherein each of said plurality of input/output control apparatuses further comprises an input/output (I/O) device.

19. (New) A computer system according to claim 18, wherein said input/output (I/O) device is connected to a peripheral device.

20. (New) A computer system according to claim 18, wherein said input/output (I/O) device is connected to a second network.